



Item

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Yeshwanth Narendar et al.

Title: METHOD FOR TREATING SEMICONDUCTOR PROCESSING
COMPONENTS AND COMPONENTS FORMED THEREBY

Application No.: 10/824,329

Filed: April 14, 2004

Examiner: Julio J. Maldonado

Group Art Unit: 2823

Atty. Docket No.: 1035-E4371

Customer No.: 34456

MS AMENDMENT
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Alexandria, VA 22313-1450

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- ☒ Form(s) PTO/SB/08A and/or PTO/SB/08B or PTO/1449
☐ Other: n/a

to the Examiner's attention in the above-identified application. Citation of such information shall not be construed as:

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2. a representation that a search has been made, other than as described below; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

For each item of information listed that is not in the English language, the undersigned has provided a concise explanation of the relevance, such as through (i) an English language abstract, (ii) an English language equivalent application, (iii) reference to discussion in the application, or (iv) if cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action that

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4

indicates the degree of relevance found by the foreign office.

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If the above-identified application is an original application filed on or after May 29, 2000:

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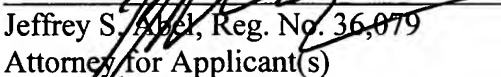
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- ☒ before the mailing date of a first Office action on the merits or before the mailing date of a first Office action after the filing of a request for continued examination under § 1.114. Therefore, no fee is believed required.
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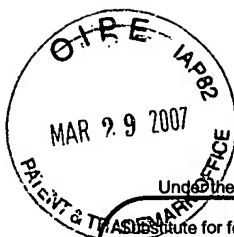
Should any PTO fees be necessary for entry of this Information Disclosure Statement, the undersigned hereby authorizes the Commissioner to charge Deposit Account 50-3797.

Date

3/26/07

Respectfully submitted,


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PTO/SB/08B (07-05)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	10/824,329
Filing Date	April 14, 2004
First Named Inventor	Yeshwanth Narendar
Art Unit	2823
Examiner Name	Julio J. Maldonado
Attorney Docket Number	1035-E4371

Sheet	1	of	1
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	A1	H. RAUH, "Atlas for Characterization of Defects in Silicon," Wacker Siltronic AG, Burghausen, Germany, pp. 1-64, 2004	
	B1	R. F. BUCKLEY et al., "Design and Analysis of a Semiconductor Wafer Processing System for 30 mm Wafers," MS Thesis - Worcester Polytechnic Institute, 12/29/99, pp 1-62	
	C1	B. LEROY et al., "Warping of Silicon Wafers," Journal Electrochemical Society, Vol. 127, No. 4, April 1980, pp. 961-970	
	D1	M. SCHREMS et al., "Simulation of Temperature Distributions During Fast Thermal Processing," Journal Electrochemical Society, Semiconductor Silicon, 1994, pp. 1050-1059	
	E1	NILSON et al., "Scaling wafer stresses and thermal processes to large wafers," Thin Solid Films 315, 1998, pp. 286-293	
	F1	VAN ZANT, "Microchip Fabrication: A Practical Guide to Semiconductor Processing," McGraw Hill, Fourth Edition, 1990, chapters 3-7	
	G1	SHIGLEY et al., "Mechanical Engineering Design," McGraw Hill, copyright 1989, p. 62, p. 159	
	H1	Machinery Handbook, 24th Edition, Industrial Press, Copyright 1992, pp. 1598-1603	
	I1		
	J1		

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